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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,352	01/15/2004	Stephen R. Van Doren	200313750-1	5314
22879 7590 03/20/2009 HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400				
EXAMINER				
DARE, RYAN A				
ART UNIT		PAPER NUMBER		
2186				
NOTIFICATION DATE		DELIVERY MODE		
03/20/2009		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/758,352

Applicant(s)

VAN DOREN ET AL.

Examiner

RYAN DARE

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-46 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-46 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SG/US)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. Pursuant to a telephone interview with Applicant on March 9, 2009, the Examiner has determined that the Notice of Non-Compliance that was issued in response to the November 21, 2008 amendment was issued in error. Therefore the Examiner has considered the 11/21/2008 amendment and examined all pending claims, 1-46.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 16-17, 27-28, 33-34, and 40-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes et al., US PGPub 2002/0184453

4. With respect to claim 1, Hughes teaches a system comprising:

a home node that provides a transaction reference to a requester in response to a request from the requester, in par.6, where the initiator is the requester, and the transaction reference is returned to the initiator.

and the requester providing an acknowledgement message to the home node in response to the transaction reference, the transaction reference enabling the requester to determine an order of requests at the home node relative to the request from the requester, in pars. 5-6,

5. With respect to claim 2, Hughes teaches the system of claim 1, wherein the home node provides a snoop associated with the request from the requester substantially in parallel with providing the transaction reference, in par. 165.

6. With respect to claim 16, Hughes teaches a multi-processor system comprising:
a first requesting processor that provides a first request for data to a home node, in pars. 5-6;

a second requesting processor that provides a second request for the data to the home node, in pars. 5-6 and

the home node comprising a transaction resource for managing requests for the data, the home providing a transaction reference message to one of the first and second requesting processors, the one of the first and second requesting processors employing the transaction reference message to ascertain a relative order of the first and second requests for the data ordered at the home node, in pars. 5-6.

7. Claim 17 is rejected using similar reasoning as claim 2.

8. With respect to claim 27, Hughes teaches a processor in a multi-processor network, the processor comprising:

a transaction structure that contains at least a first entry associated with a first request for data issued by the processor, the first entry including a transaction reference field that has a value based on a transaction reference message from a home node for the data, the value of the transaction reference field providing an indication of an order of transactions for the data at the home node, in pars. 5-6; and

a controller that controls how to respond to a second request for the data received from the home node based on the value of the transaction reference field, in pars. 5-6.

9. Claim 28 is rejected using similar reasoning as claim 2.

10. With respect to claim 33, Hughes teaches a multi-processor system comprising:
means for providing a transaction reference message substantially in parallel with at least one snoop request from a home node in response to a first request for data from a requesting processor, in pars. 5-6;

means for setting a transaction reference field at the requesting processor in response to the transaction reference message, in pars. 5-6; and

means for responding to at least a second request provided to the requesting processor based on a condition of the transaction reference field when the at least a second request is received, in pars. 5-6.

11. Claim 34 is rejected using similar reasoning as claim 2.

12. With respect to claim 40, Hughes teaches a method comprising:

providing a fill marker message from a home node in response to a first request for a block of data from a requester, in pars. 5-6;

setting a fill marker status field at the requester in response to the fill marker message from the home node, in pars. 5-6; and

providing a response from the requester to a second request for the block of data that varies temporally based on a condition of the fill marker status field at the requester, in pars. 5-6.

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13. Claim 41 is rejected using similar reasoning as claim 2.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 3-15, 18-26, 29-32, 35-39 and 42-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes as applied to claims 1, 16, 27, 33, and 40 above, in view of Van Loo, US Patent 5,657,472.

17. With respect to claim 3, Hughes teaches all limitations of the parent claim, but fails to teach the system of the present claim. Van Loo teaches the system of claim 1, wherein the system employs a null-directory cache coherency protocol, the home node providing a transaction reference for each request to the home node, in col. 10, lines 44-45.

18. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

19. With respect to claim 4, Hughes teaches all limitations of the parent claim, but fails to teach the system of the present claim. Van Loo teaches the system of claim 1, wherein the system employs a directory-based cache coherency protocol, the home node providing a transaction reference for a selected subset of requests to the home node, in col. 1, lines 38-41.

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

21. With respect to claim 5, Van Loo teaches the system of claim 4, wherein the selected subset of requests to the home node comprises write requests and requests in response to which the home node generates at least one snoop, in col. 21, lines 48-61.

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van

Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

23. With respect to claim 6, Hughes teaches the system of claim 4, wherein the requester is configured to employ data received in response to the request from the requester for a single use, in pars. 5-6. Van Loo teaches that if the requester receives an invalidate command before receiving a copy of the data in response to the request from the requester and when a transaction reference has not yet been received by the requester, in col. 22, lines 46-55.

24. With respect to claim 7, Hughes teaches all limitations of the parent claim, but fails to teach the system of the present claim. Van Loo teaches the system of claim 1, wherein the home node further comprises a transaction resource that maintains transaction information associated with each of a plurality of requests to the home node, the transaction information including an indication of whether the requester has received the transaction reference associated with the request from the requester and an indication of whether a response has been received for each snoop issued by the home node in response to the request from the requester., in col. 15, lines 48-61.

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

26. With respect to claim 8, Hughes teaches all limitations of the parent claim, but fails to teach the system of the present claim. Van Loo teaches the system of claim 1, wherein the requester comprises a first requester that provides a first request for data to the home node, the system further comprising a second requester that provides a second request for the data to the home node, the home node receiving the second request for the data subsequent to the first request for the data, in col. 71, lines 12-29.

27. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

28. With respect to claim 9, Van Loo teaches the system of claim 8, wherein the home node is programmed to issue a transaction reference associated with the second request based on transaction information at the home node associated with the first request indicating that the first request from has been completed, in col. 71, lines 30-39.

29. With respect to claim 10, Van Loo teaches the system of claim 9, wherein the transaction information at the home node associated with the first request further comprises an indication that the transaction reference has been received by the first requester and an indication that the home node has received a complete set of at least one response to each of at least one snoop provided by the home node in response to the first request, in col. 71, lines 12-39.

30. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

31. With respect to claim 11, Hughes teaches all limitations of the parent claim, but fails to teach the system of the present claim. Van Loo teaches the system of claim 1, wherein the requester further comprises a processor having a miss address file that includes an entry associated with the request from the requester, wherein a transaction reference field in the entry associated with the request from the requester is set in response to the transaction reference from the home node, in col. 71, lines 30-39.

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

33. With respect to claim 12, Van Loo teaches the system of claim 11, wherein the processor further comprises a queue, the requester controlling whether a snoop for data from the home node is placed in the queue based on the transaction reference field. in col. 71, lines 12-39.

34. With respect to claim 13, Van Loo teaches the system of claim 12, wherein the processor further comprises an associated cache that includes a plurality of cache lines,

the requester is configured to provide a response to the snoop for the data from the home node based on a present state of the data in a respective one of the cache lines if the transaction reference field is not set when the snoop for the data from the home node is received by the requester, in col. 11, line 59 through col. 12, line 27.

35. With respect to claim 14, Van Loo teaches the system of claim 12, wherein the processor further comprises an associated cache that includes a plurality of cache lines, the requester is configured to place the snoop for the data from the home node in the queue for deferring a response if the transaction reference field is set when the snoop for the data from the home node is received by the requester, in col. 11, line 59 through col. 12, line 27.

36. With respect to claim 15, Hughes teaches all limitations of the parent claim, but fails to teach the system of the present claim. Van Loo teaches the system of claim 1, wherein the system comprises an unordered network, in col. 15, lines 10-28.

37. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes and Van Loo before him at the time the invention was made, to modify the memory request system of Hughes with the memory request system of Van Loo in order to reduce latency experienced by data processors during memory transactions, as taught by Van Loo in col. 2, lines 4-8.

38. With respect to claims 18-26, they claim similar features as claims 3-15 but depend from claim 16, and are therefore rejected using similar logic.

39. With respect to claims 29-32, they claim similar features as claims 3-15 but depend from claim 27, and are therefore rejected using similar logic.

40. With respect to claims 35-39, they claim similar features as claims 3-15 but depend from claim 33, and are therefore rejected using similar logic.

41. With respect to claims 42-46, they claim similar features as claims 3-15 but depend from claim 40, and are therefore rejected using similar logic.

Response to Arguments

42. Applicant's arguments, see amendments, filed 11/21/2008, with respect to the rejection(s) of claim(s) 1-46 under 35 USC 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hughes, as discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN DARE whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan Dare/
March 16, 2009

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

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